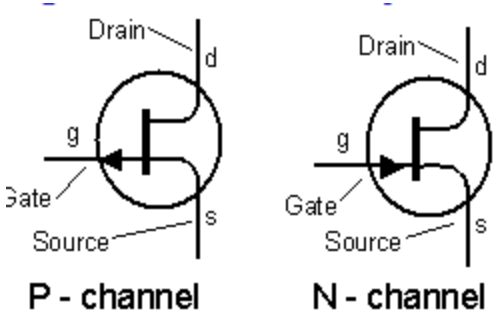
Field-Effect Transistors

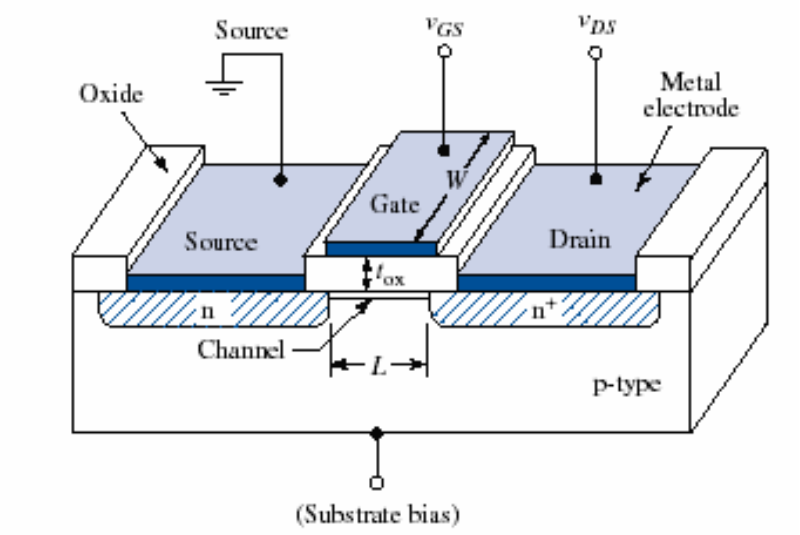
The **field-effect transistor** (**JFET)** is the simplest type of field effect transistors.

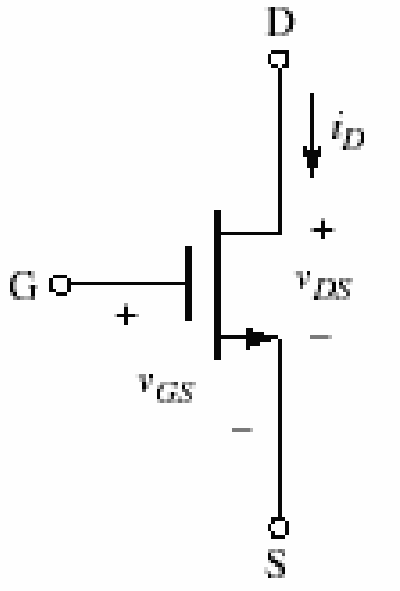
- Structure
- Current-voltage Characteristics
- MOSFET as an Amplifier
- CMOS
- The CMOS Digital Logic Inverter



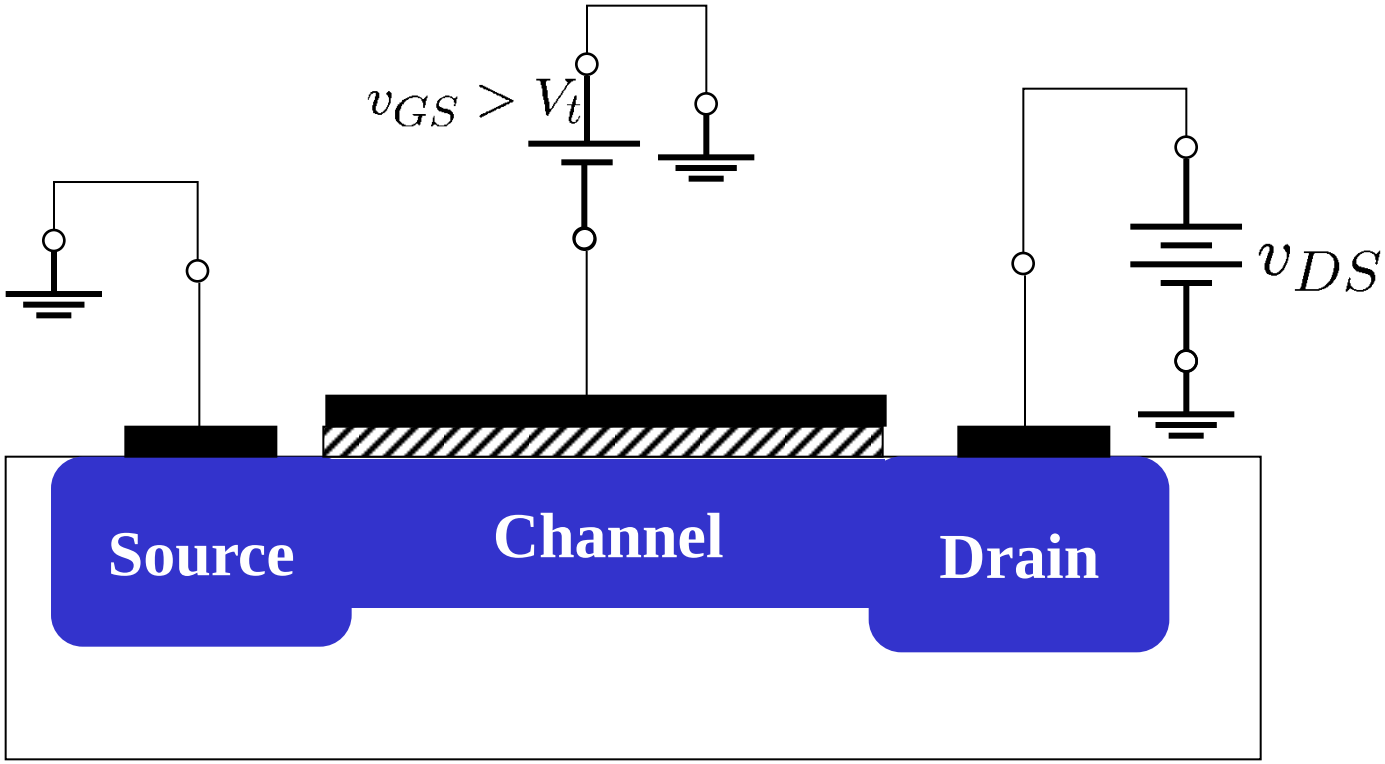
n-channel Enhancement mode MOSFET

Two n-regions called **source** terminal and **drain** terminal. The current in a MOSFET is the result of flow of charge in the inversion layer called the channel region.





For $v_{DS} <<$



The channel width is uniform

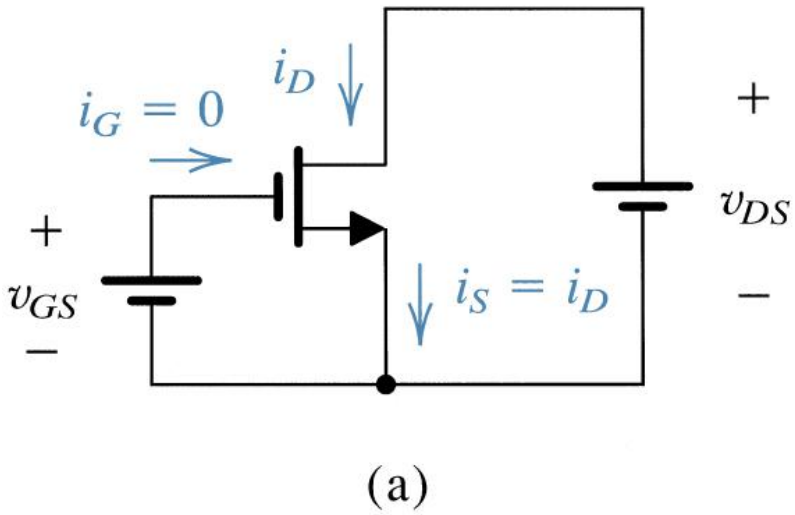
i_D-v_{DS} Characteristics

Cutoff; **Triode (**switch**)**; and **Saturation (**amplifier**)** regions

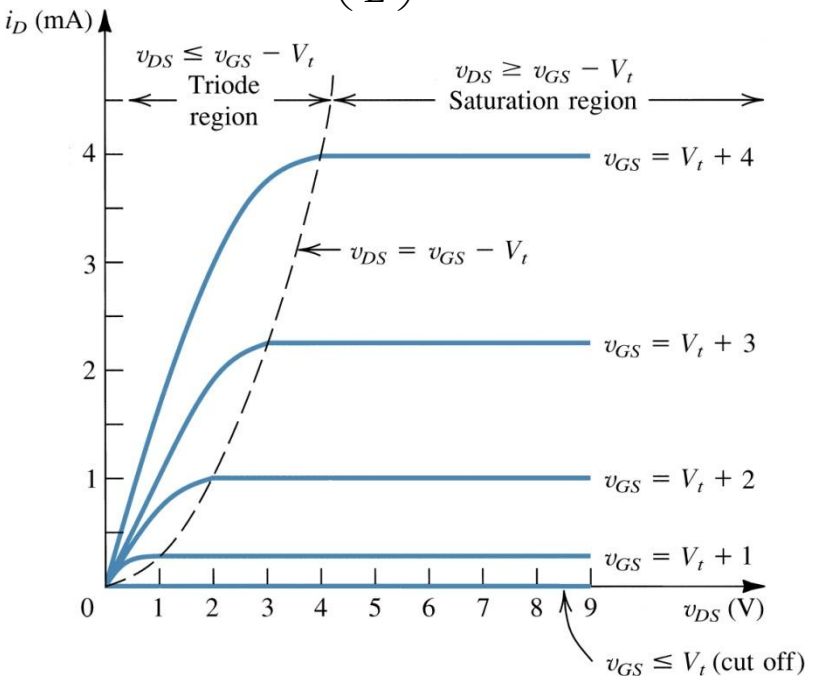
$v_{GS} \geq V_t$ (Induced Channel)

$V_t = 1\,\text{V}$

$k'_n \left(\frac{W}{L}\right) = 0.5\,\text{mA/V}^2$



(a)



To operate the MOSFET in the **triode** region

$$v_{DS} \langle v_{GS} - V_t$$

$$i_D = k'_n \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v^2{}_{DS}\right]$$

$$i_D = k'_n \frac{W}{L}(v_{GS} - V_t)v_{DS}$$

$$r_{DS} = \frac{v_{DS}}{i_D} = \left[k'_n \frac{W}{L}(v_{GS} - V_t)\right]^{-1}$$

To operate the MOSFET in the saturation region

$$v_{GS} \geq V_t$$

$$v_{GD} \leq V_t$$

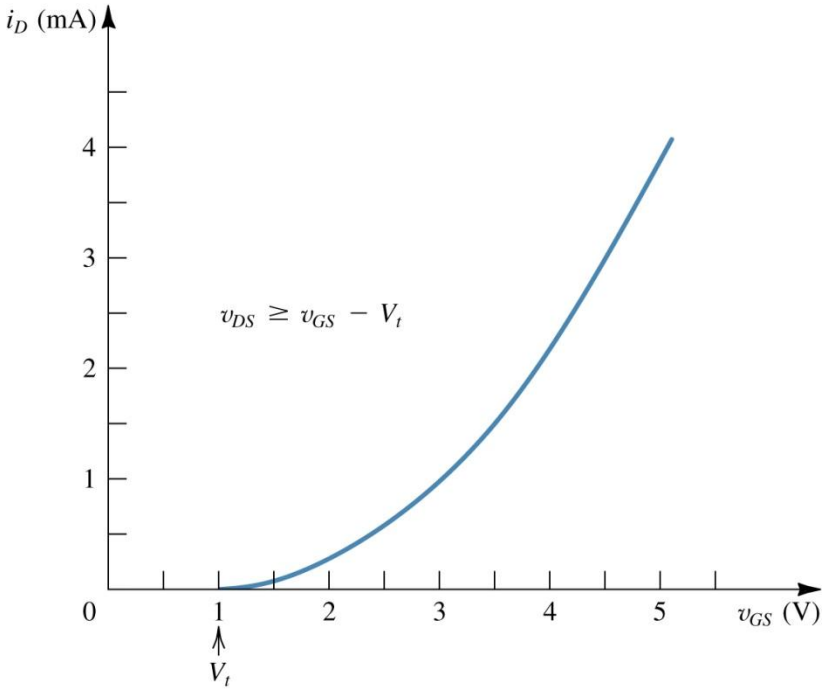
$$v_{DS} \geq v_{GS} - V_t$$

$$v_{DS} = v_{GS} - V_t$$

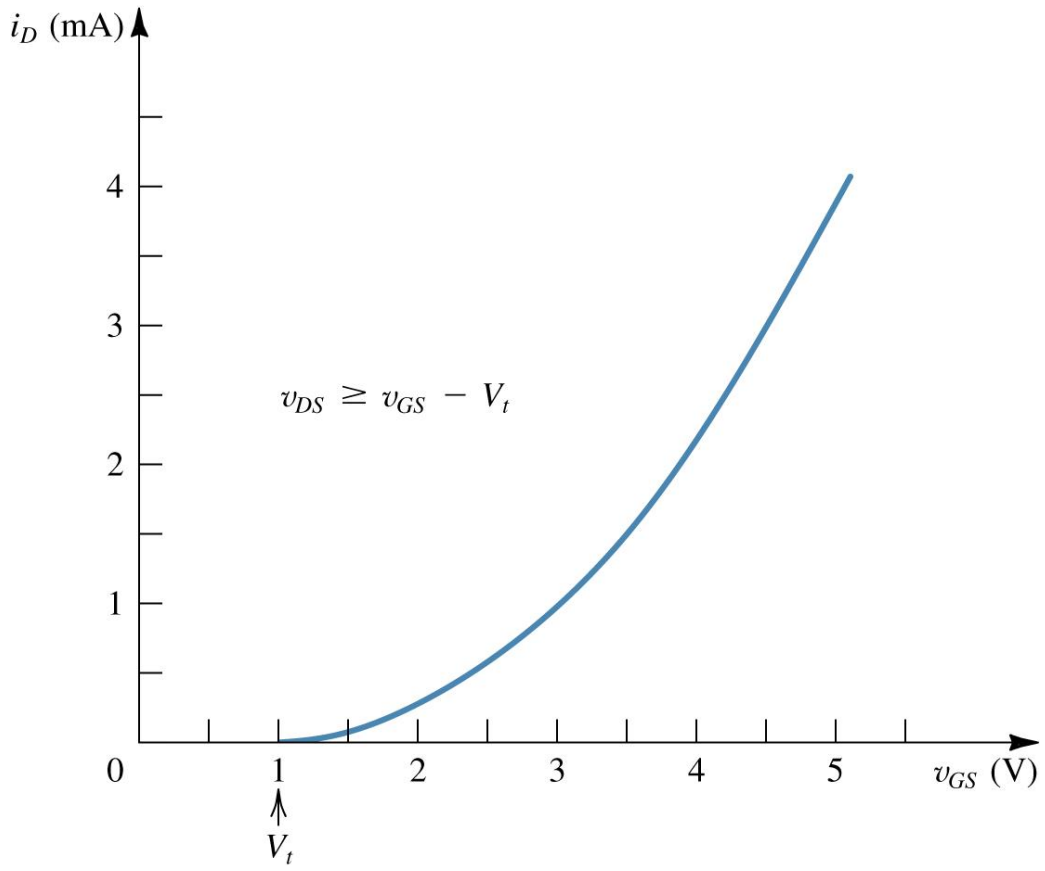
$$i_D = \frac{1}{2} k'_n \frac{W}{L} v^2_{DS}$$

$$i_D = \frac{1}{2} k'_n \frac{W}{L} v^2_{DS}$$

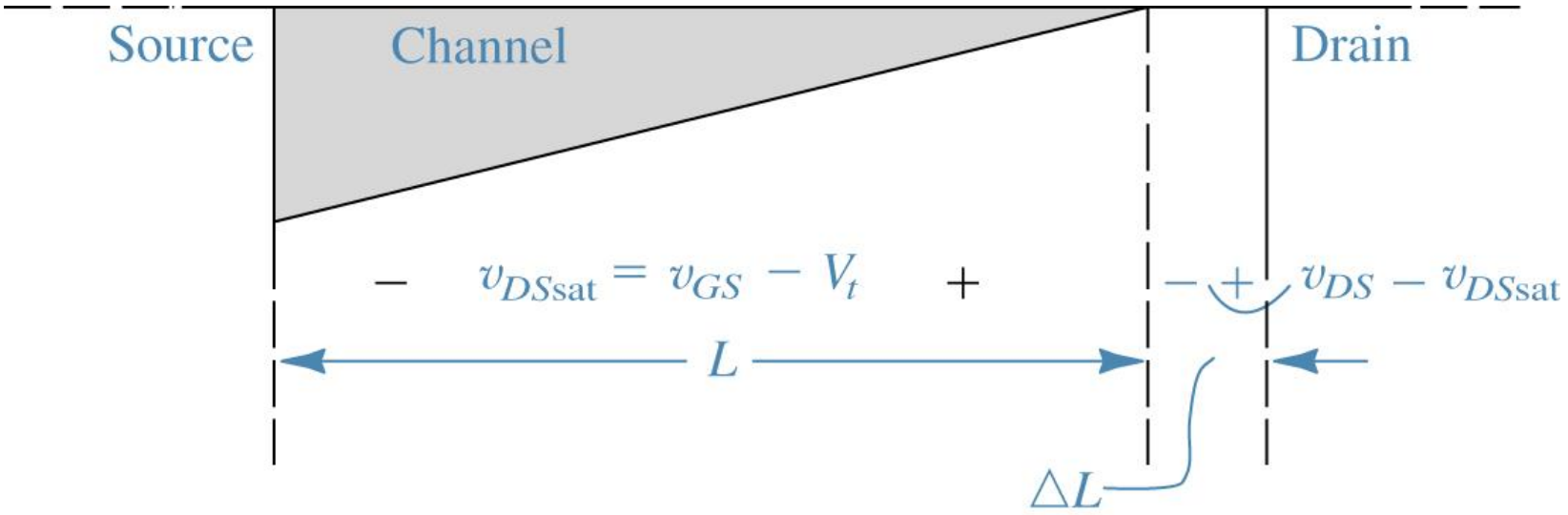
i_D - v_{GS} Characteristics
for an enhancement - type NMOS transistor in Saturation
(V_t = 1 V, k' nW/L = 0.5 mA/V2)



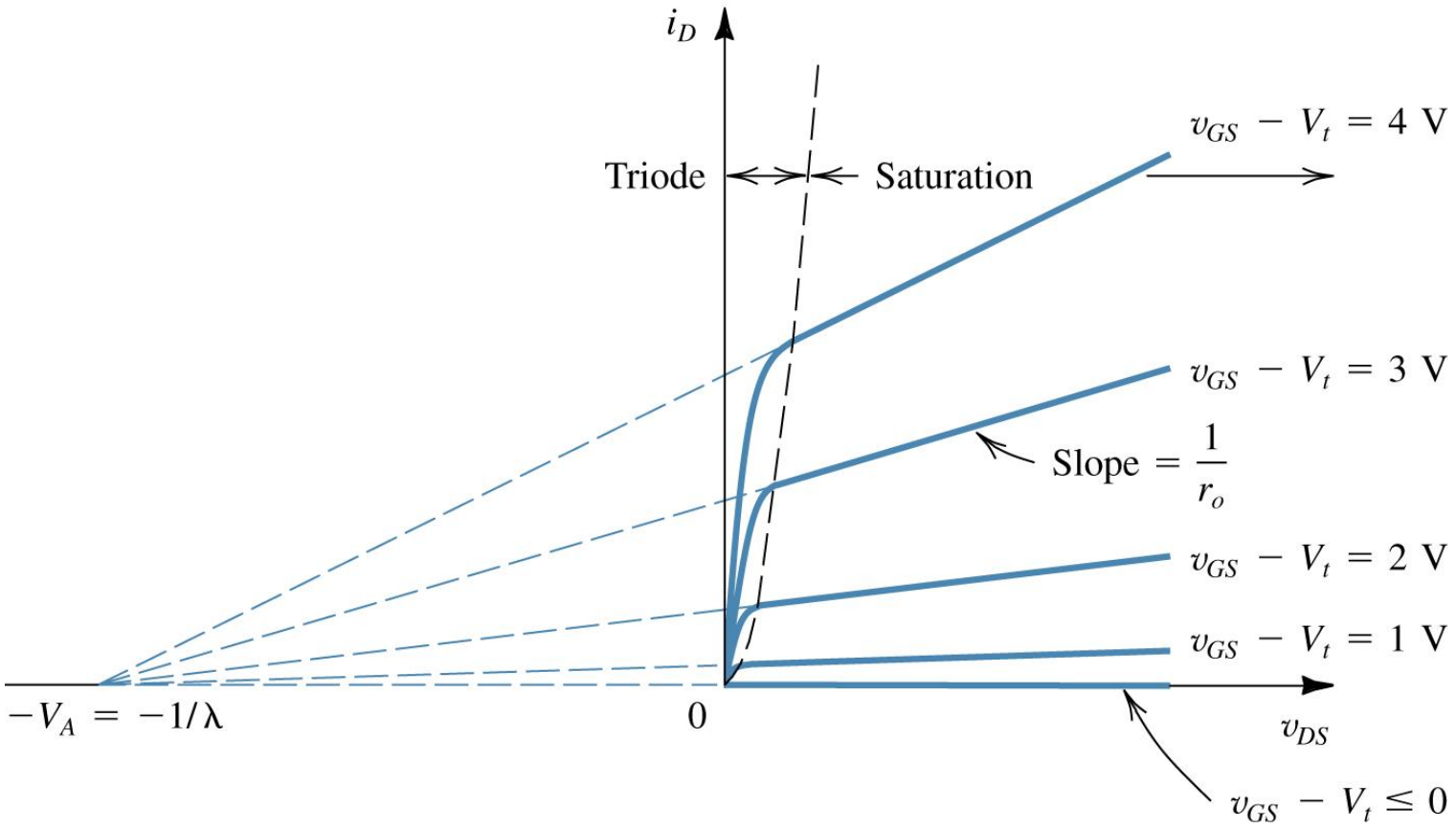
i_D-v_{GS} characteristics for an enhancement-type NMOS transistor in Saturation (V_t= 1 V, k'$_n$*W/L*=0.5 mA/V^2)



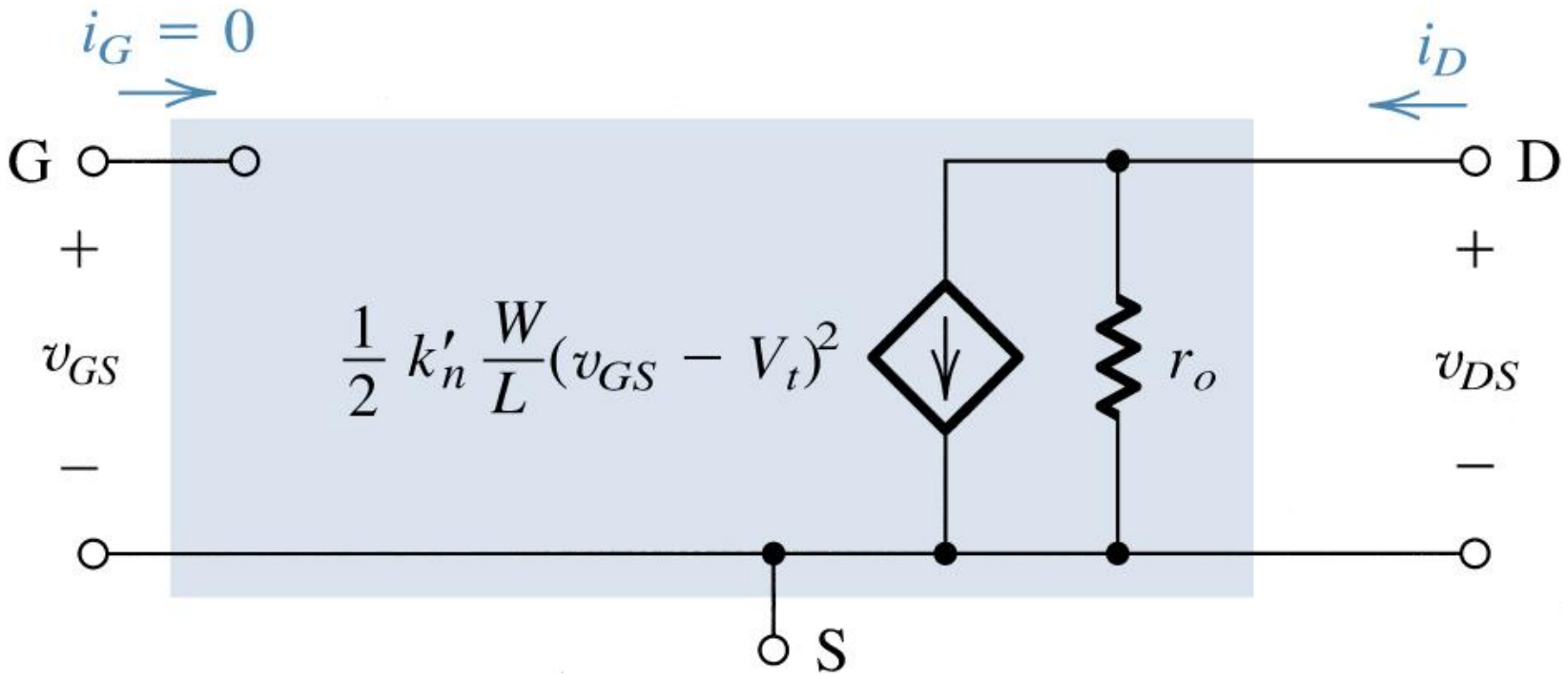
Increasing v_{DS} beyond v_{Dsat} causes the channel pinch-off to move away from the drain.



Effect of v_{DS} on i_D in the saturation region



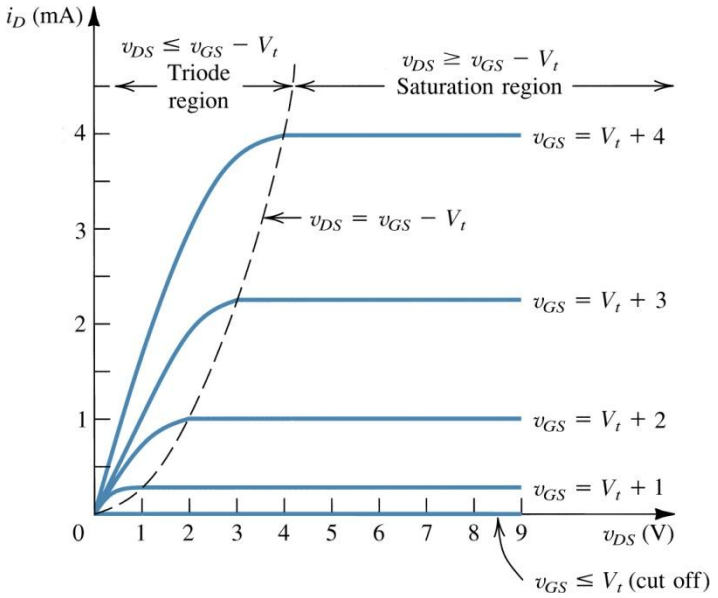
Large-signal equivalent circuit model of the **n**-channel MOSFET in saturation.



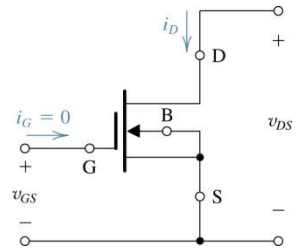
Exercise 5.3

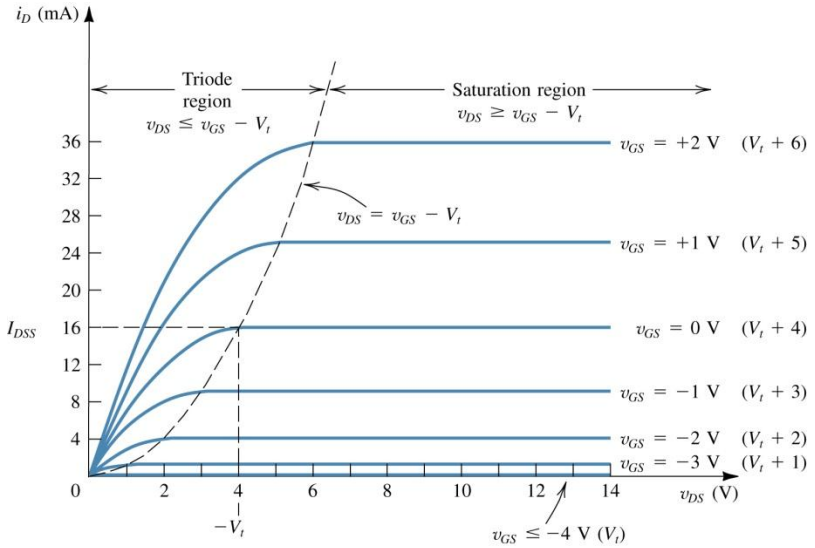
- An Enhancement-type NMOS transistor with V_t = 2 V has its source terminal grounded and a 3-V DC source connected to the gate. In what region of operation does the device operate for:

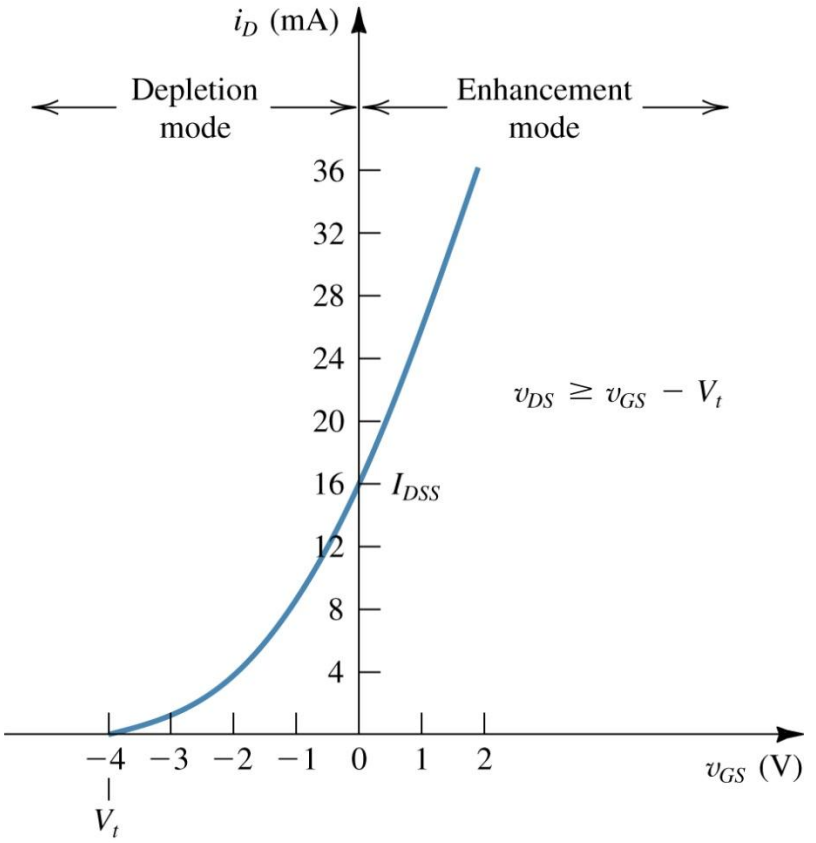
- V_D = +0.5 V ($v_{DS} \leq v_{GS}$-V_t: Triode)
- V_D = 1 V ($v_{DS} \geq v_{GS}$-V_t: Saturation)
- V_D = 5 V ($v_{DS} \geq v_{GS}$-V_t: Saturation)



The Current-Voltage Characteristics of the Depletion n-Channel MOSFET for Which V_t = -4V and $k'_n W/L$ = 2 mA/V^2







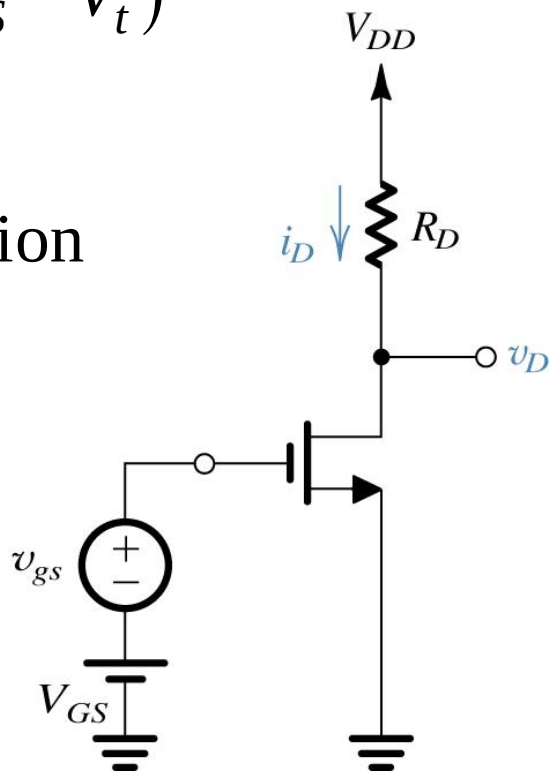
The MOSFET as an Amplifier
DC Bias

$$I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_t)^2$$

$$V_D = V_{DD} - R_D I_D$$

To Ensure Saturation

$$V_D \rangle V_{GS} - V_t$$



The Signal Current in the Drain Terminal

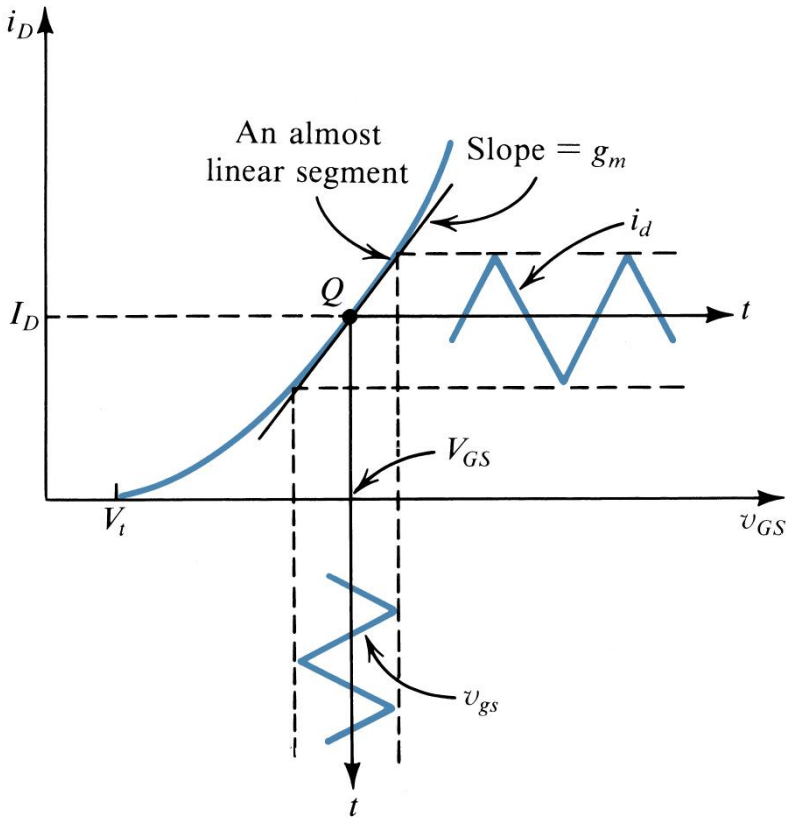
$$v_{GS} = V_{GS} + v_{gs}$$

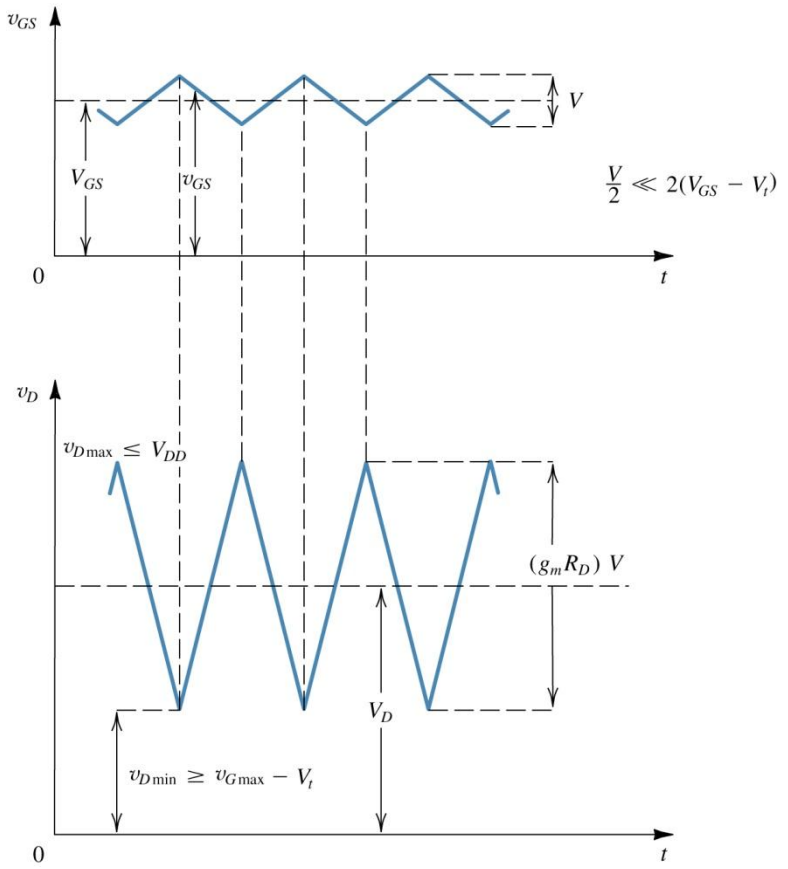
$$i_D = \frac{1}{2} k'_n \frac{W}{L} \left(V_{GS} + v_{gs} - V_t\right)^2$$

$$i_D = I_D + i_d$$

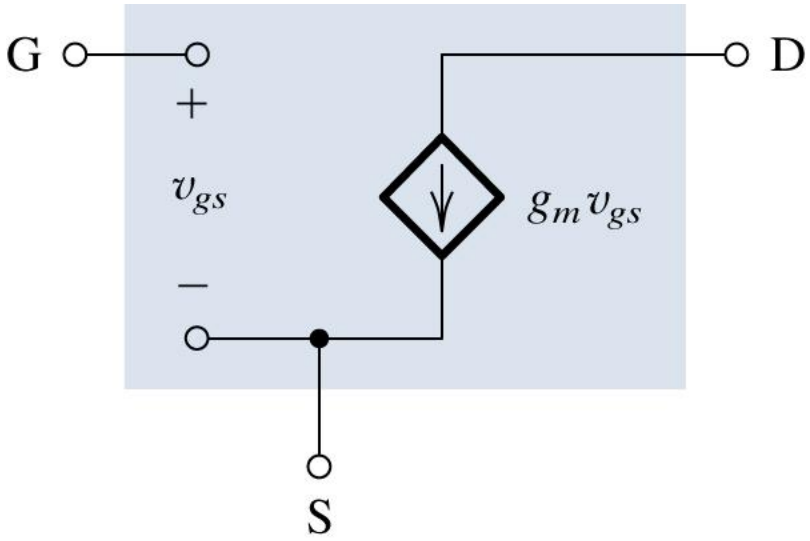
$$i_d = k'_n \frac{W}{L} \left(V_{GS} - V_t\right) v_{gs}$$

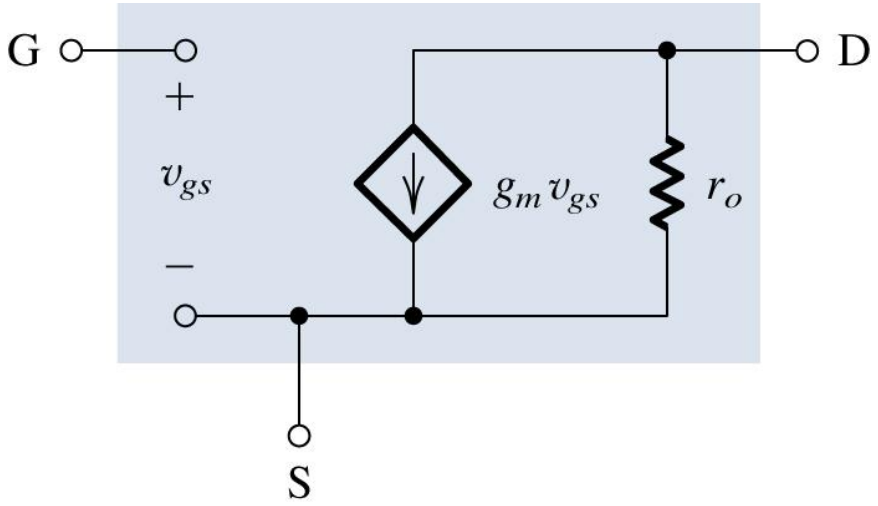
$$g_m = \frac{i_d}{v_{gs}} = k'_n \frac{W}{L} \left(V_{GS} - V_t\right)$$



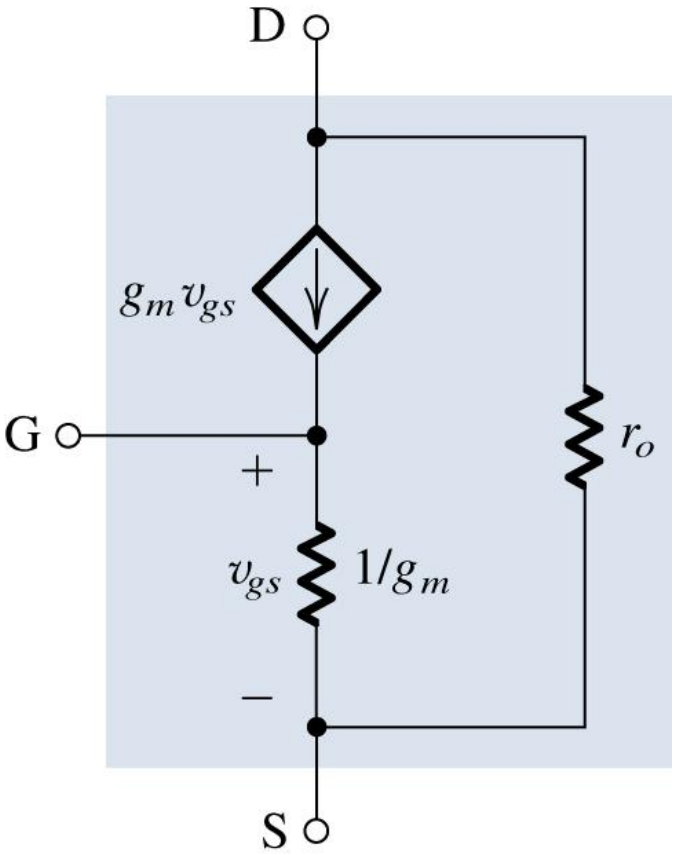

v_{GS}
V
V_{GS}
v_{GS}
$\frac{V}{2} \ll 2(V_{GS} - V_t)$
0
t
v_D
$v_{D\max} \leq V_{DD}$
$(g_m R_D)\, V$
V_D
$v_{D\min} \geq v_{G\max} - V_t$
0
t

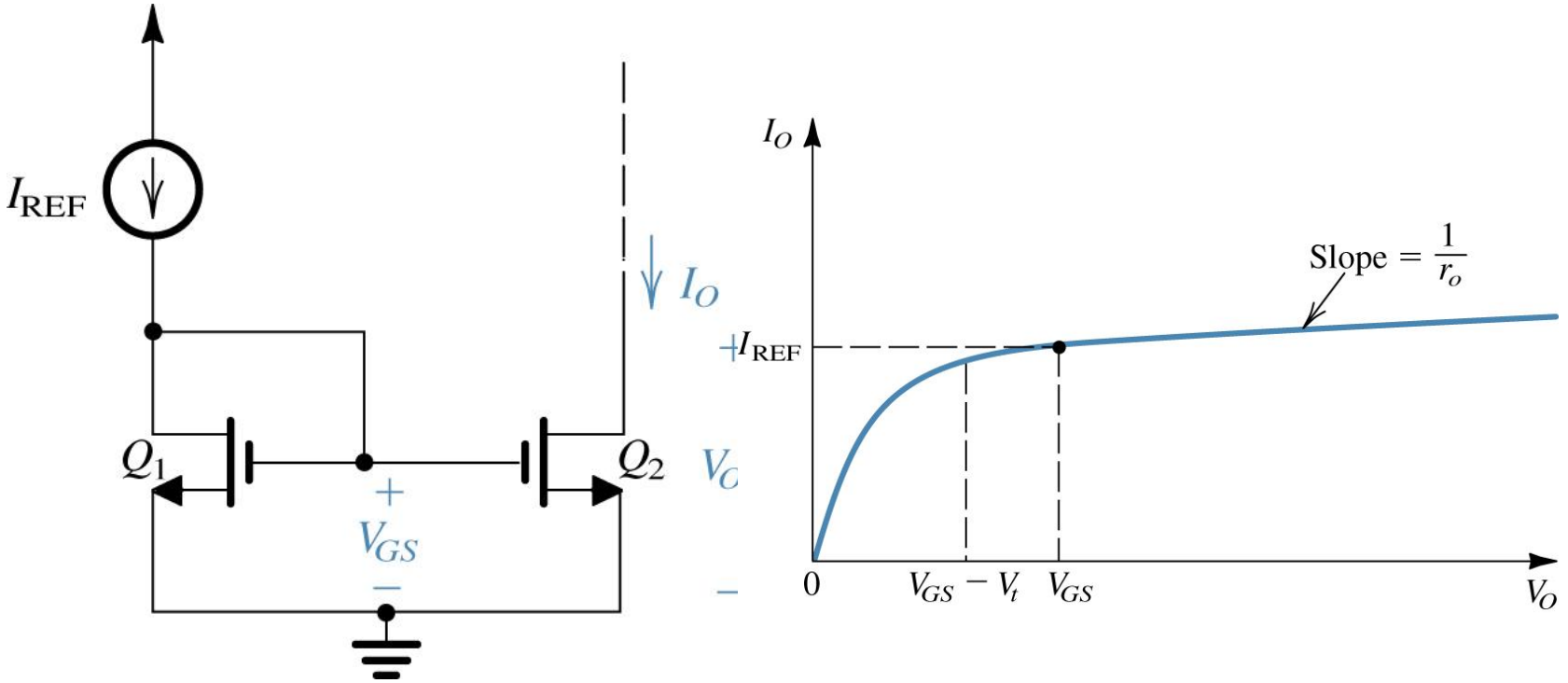
Small Signal Equivalent Circuit





The T Model




I_{REF}
I_O
Q_1
Q_2
V_{GS}
+
−
V_O
I_O
I_{REF}
Slope = $\frac{1}{r_o}$
0
$V_{GS} - V_t$
V_{GS}
V_O

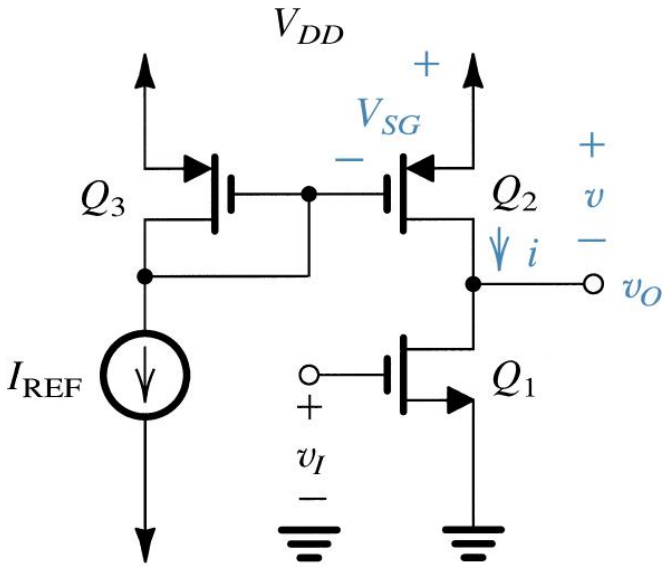
Basic Configurations of Single-Stage IC MOS Amplifiers

- Common Source (CS)
- Common Gate (CG)
- Common Drain (CD)

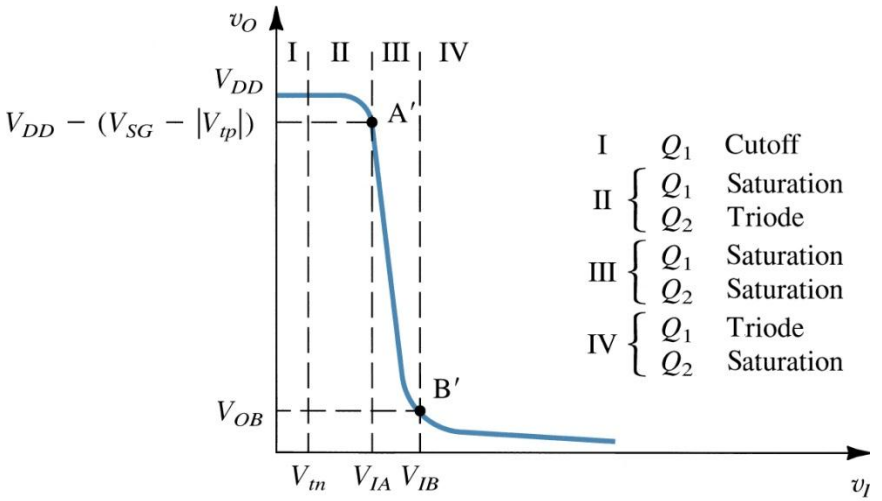
CMOS Common-Source Amplifier

$$r_{o2} = \frac{|V_{A2}|}{I_{REF}}$$

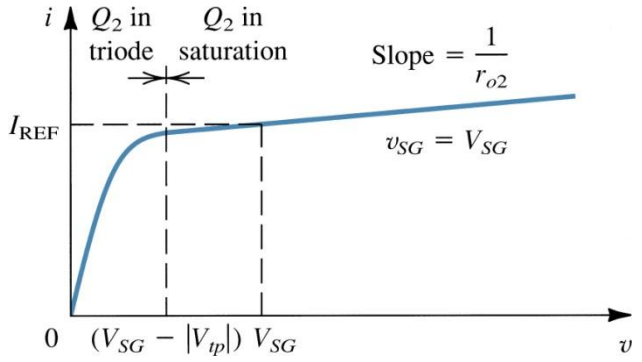
$$A_v = \frac{v_o}{v_i} = -g_m(r_{o1} // r_{o2})$$



(a)



(d)

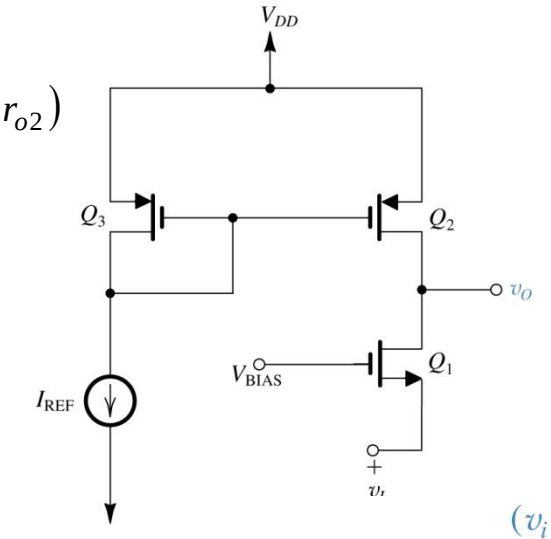


The CMOS Common-Gate Amplifier

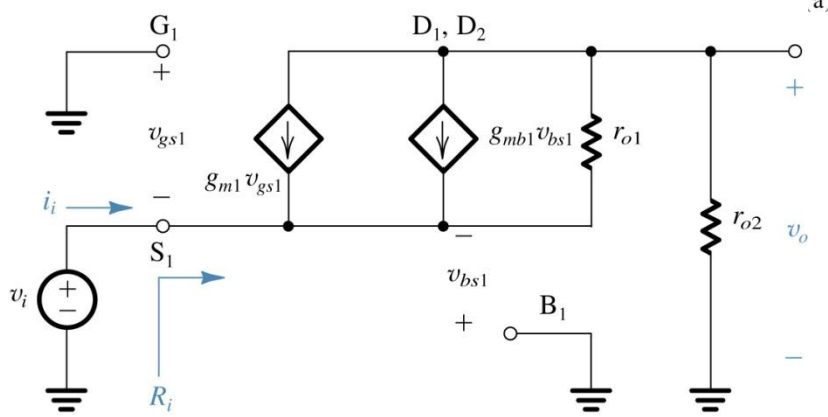
$$A_v = \frac{v_o}{v_i} = \left(g_{m1} + g_{mb1} + \frac{1}{r_{o1}} \right)(r_o \,//\, r_{o2})$$

$$A_v \cong (g_{m1} + g_{mb1})(r_{o1} \,//\, r_{o2})$$

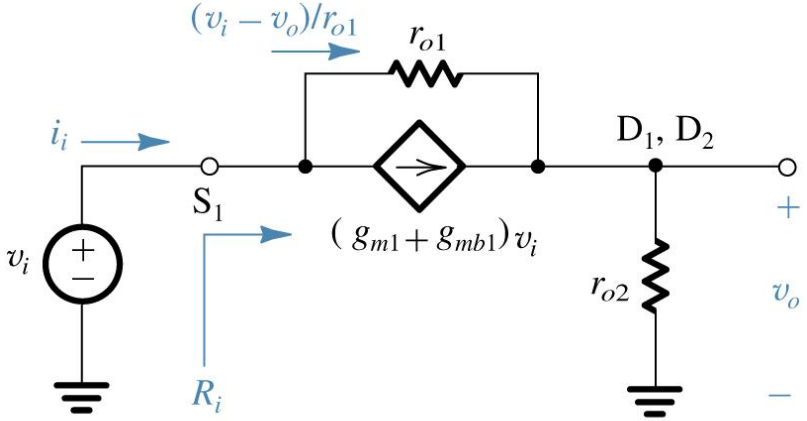
$$Ri \cong \frac{v_i}{i_i} \approx \frac{1}{(g_{m1} + g_{mb1})}\left(1 + \frac{r_{o2}}{r_{o1}}\right)$$



(a)

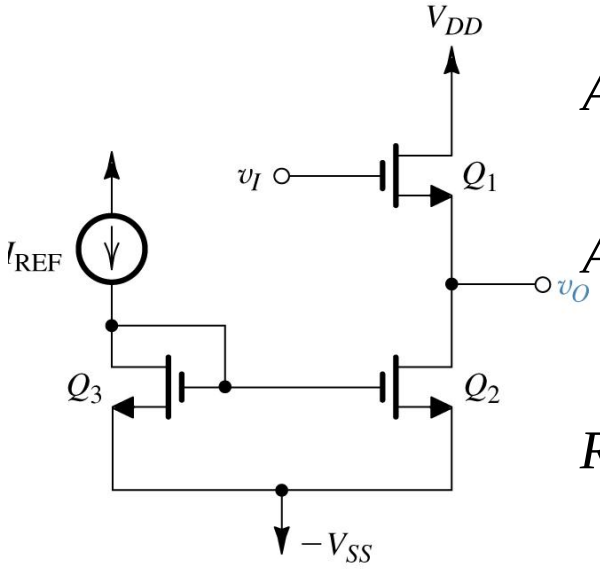


(b)



(c)

The Common-Drain or Source-Follower Amplifier

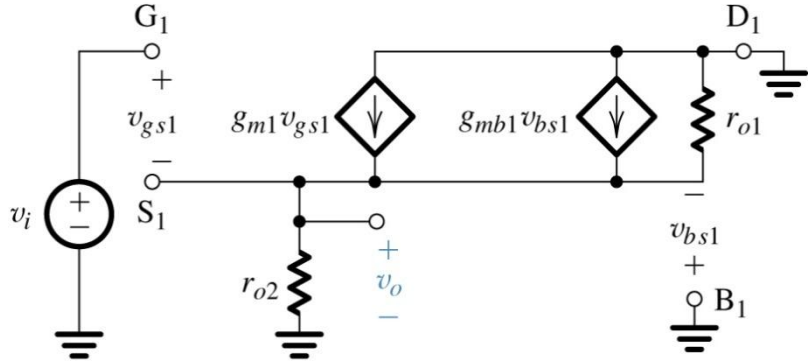


(a)

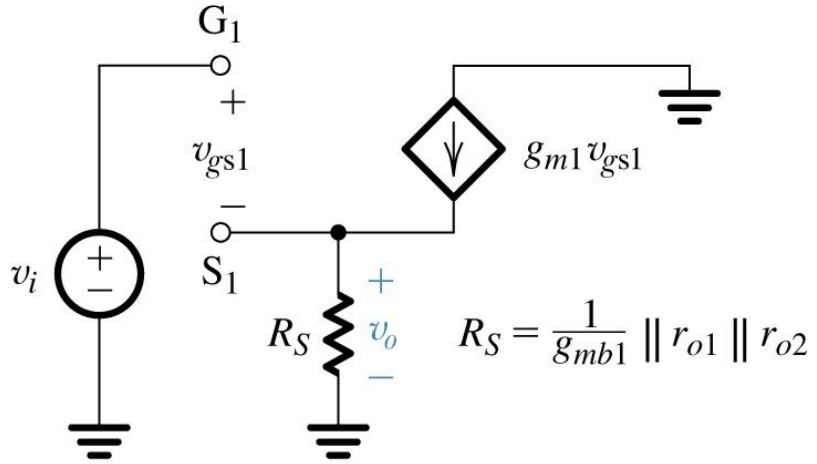
$$A_v = \frac{v_o}{v_i} = \frac{g_{m1}R_S}{1+g_{m1}R_S}$$

$$A_v = \frac{g_{m1}}{g_{m1}+g_{mb1}+\dfrac{1}{r_{o1}}+\dfrac{1}{r_{o2}}} = \frac{g_{m1}}{g_{m1}+g_{mb1}}$$

$$R_o = (1/g_{m1})//(1/g_{mb1})//r_{o1}//r_{o2}$$

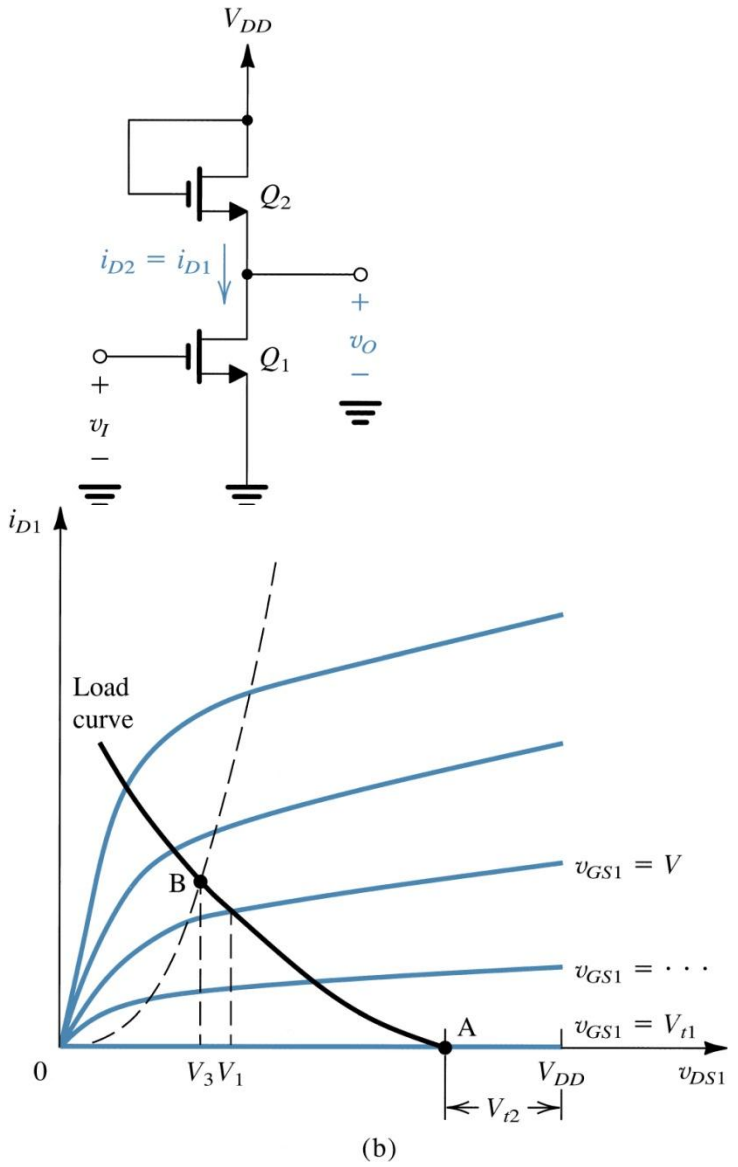


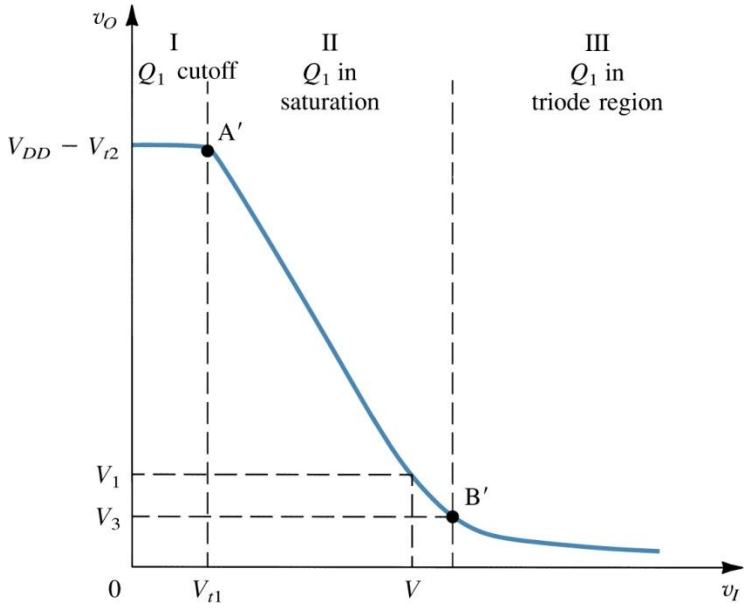
(b)



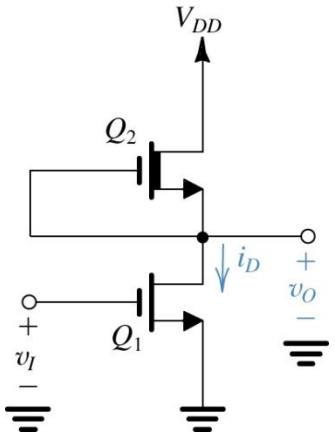
(c)

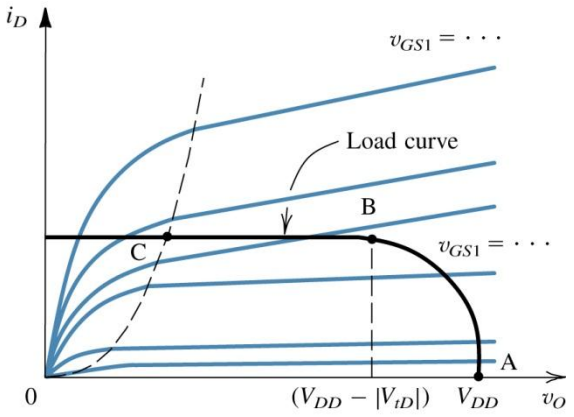
NMOS Amplifier with Enhancement Load

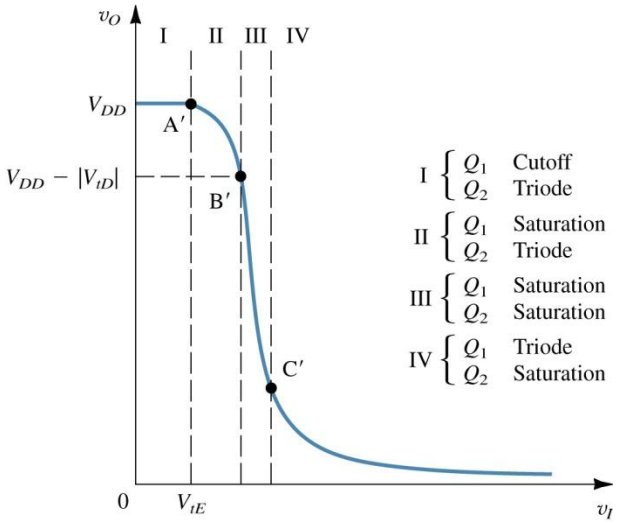




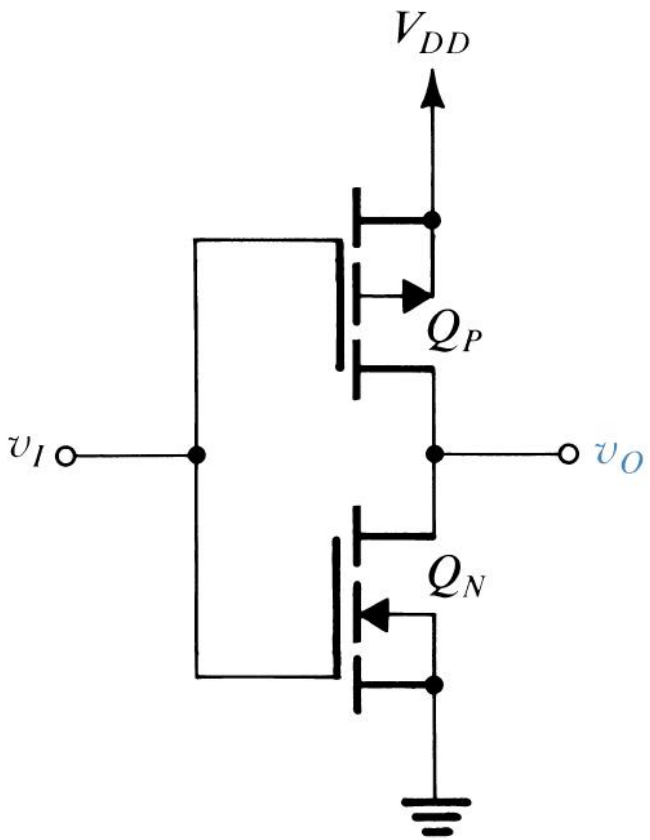
The NMOS Amplifier with Depletion Load

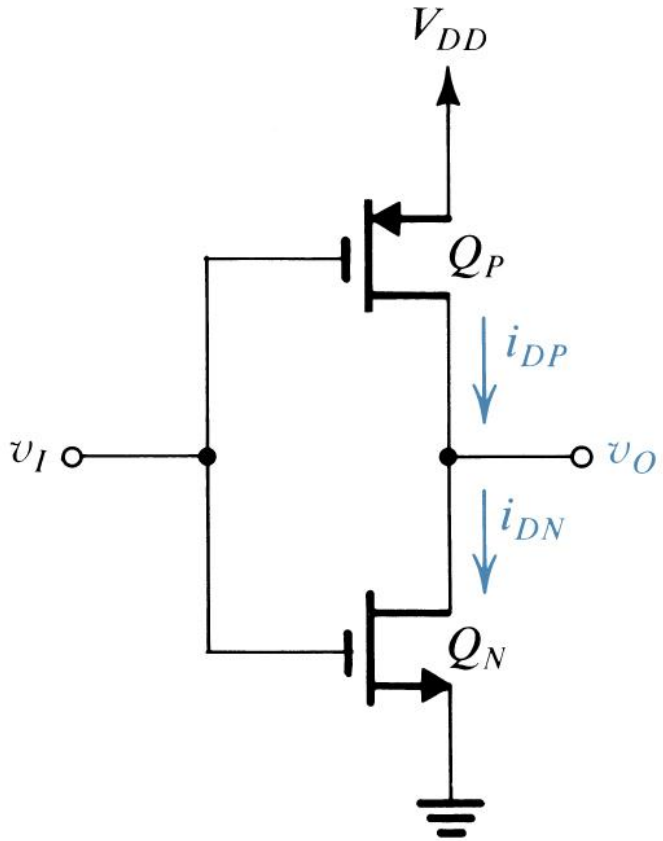




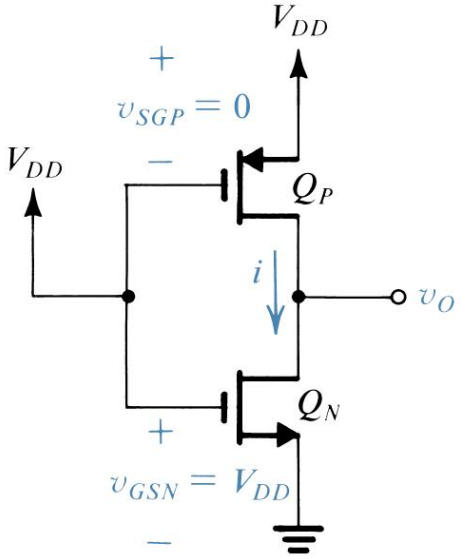


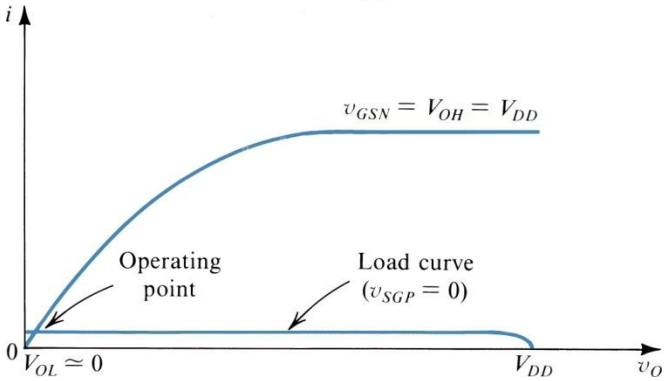
CMOS Inverter

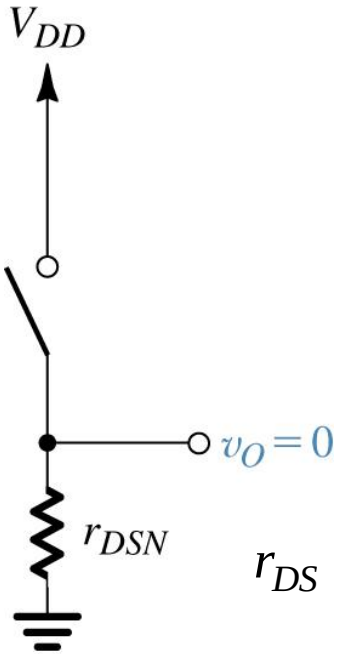




Operation of the CMOS Inverter When v_I is High



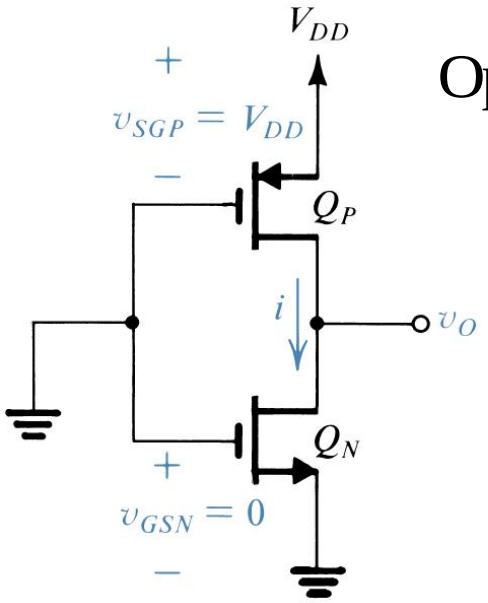


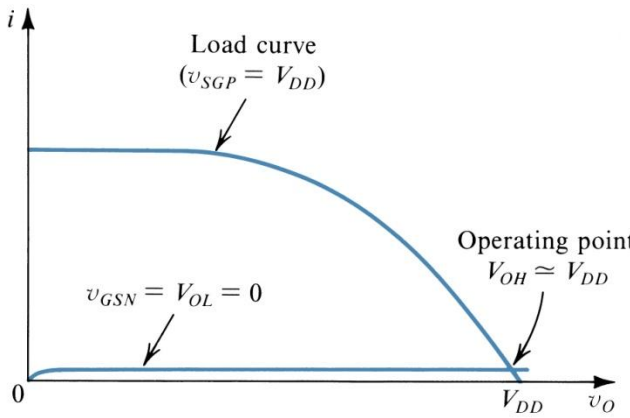


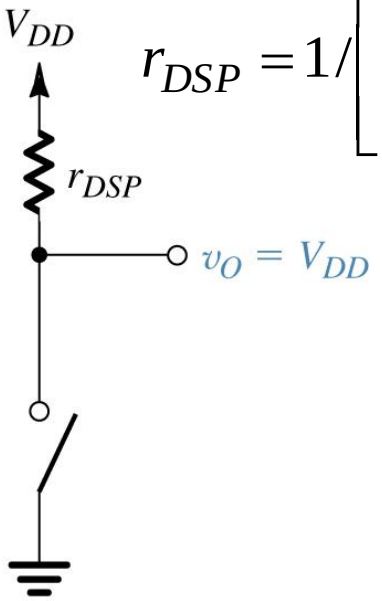
$$r_{DS} = 1/\left[k'_n \left(\frac{W}{L} \right)_n \left(V_{DD} - V_{tn} \right) \right]$$

(c)

Operation of the CMOS Inverter When v_I is Low



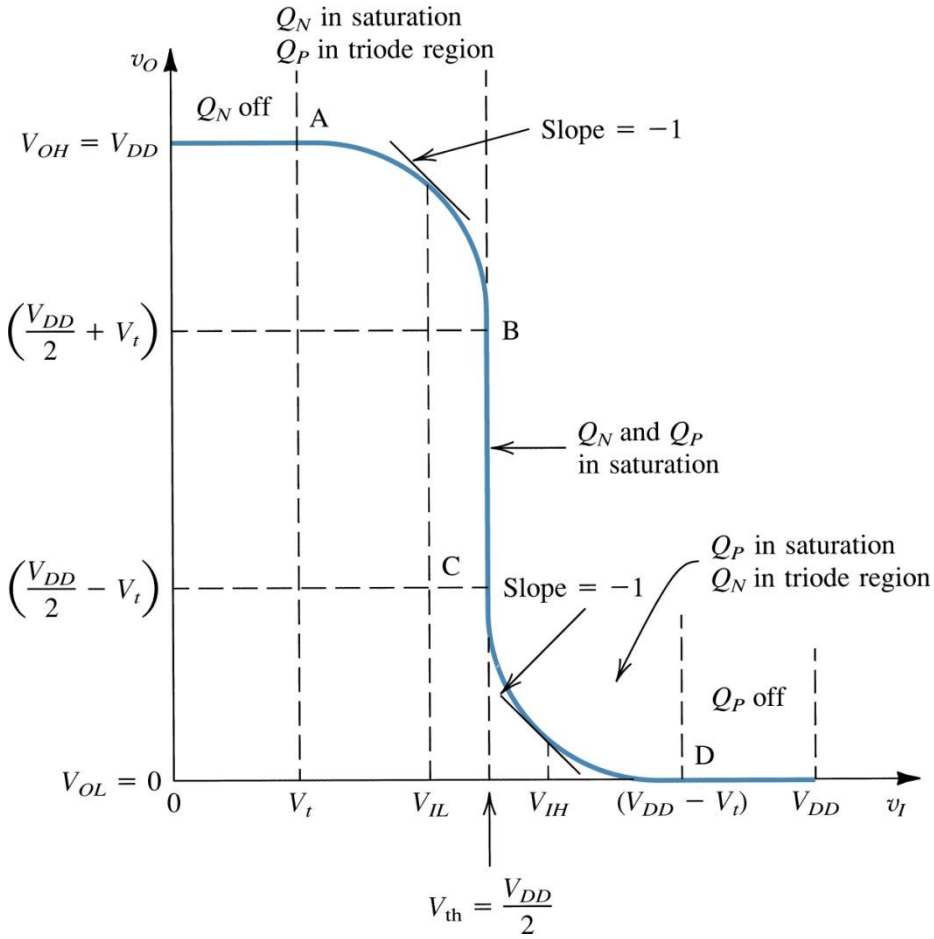




$$r_{DSP} = 1/\left[k'_p \left(\frac{W}{L} \right)_p \left(V_{DD} - |V_{tp}| \right) \right]$$

(c)

The Voltage Transfer Characteristics of the CMOS Inverter and Noise Figures



$$V_{IH} = \frac{1}{8}\left(5V_{DD} - 2V_t\right)$$

$$V_{IL} = \frac{1}{8}\left(3V_{DD} + 2V_t\right)$$

$$N_{MH} = V_{OH} - V_{IH}$$

$$N_{ML} = V_{IL} - V_{OL}$$

$$V_{th} = \frac{r\left(V_{DD} - \left|V_{tp}\right|\right) + V_{th}}{1 + r}$$

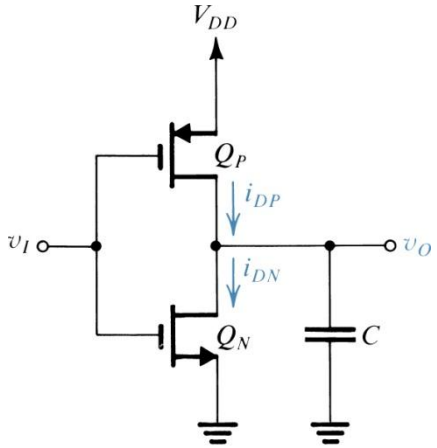
$$r = \sqrt{\frac{k'_p \left(W/L\right)_p}{k'_n \left(W/L\right)_n}}$$

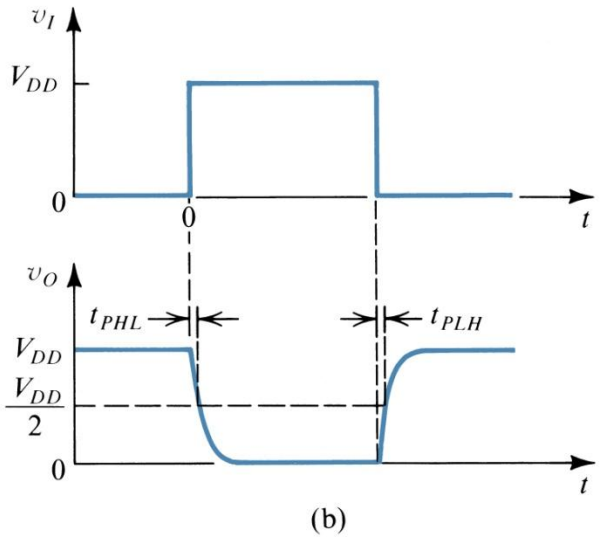
Dynamic Operation

$$t_{PHL} = \frac{1.6C}{k'_n (W/L)_n V_{DD}} \text{(High to Low)}$$

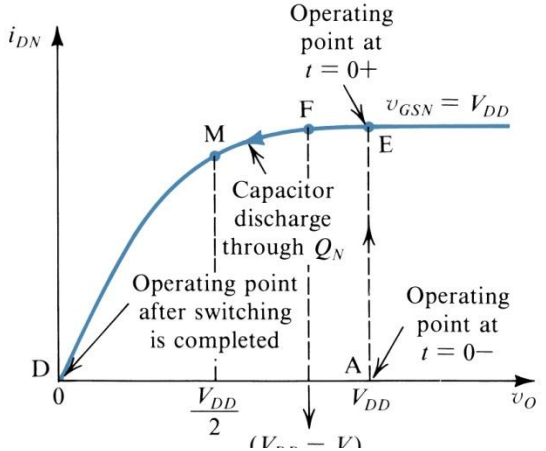
$$t_{PLH} = \frac{1.6C}{k'_n (W/L)_p V_{DD}} \text{(Low to High)}$$

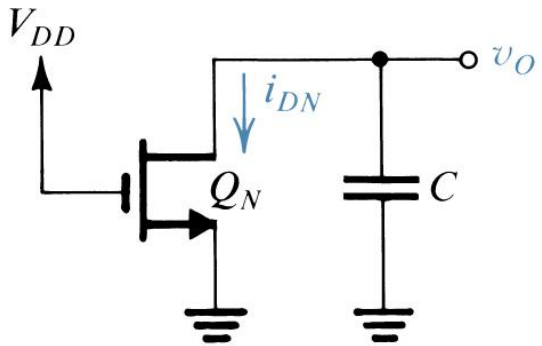
$$t_p = \frac{t_{PHL} + t_{PLH}}{2} \text{(Propagation Delay)}$$





(b)





(d)