Operational Amplifier Circuits

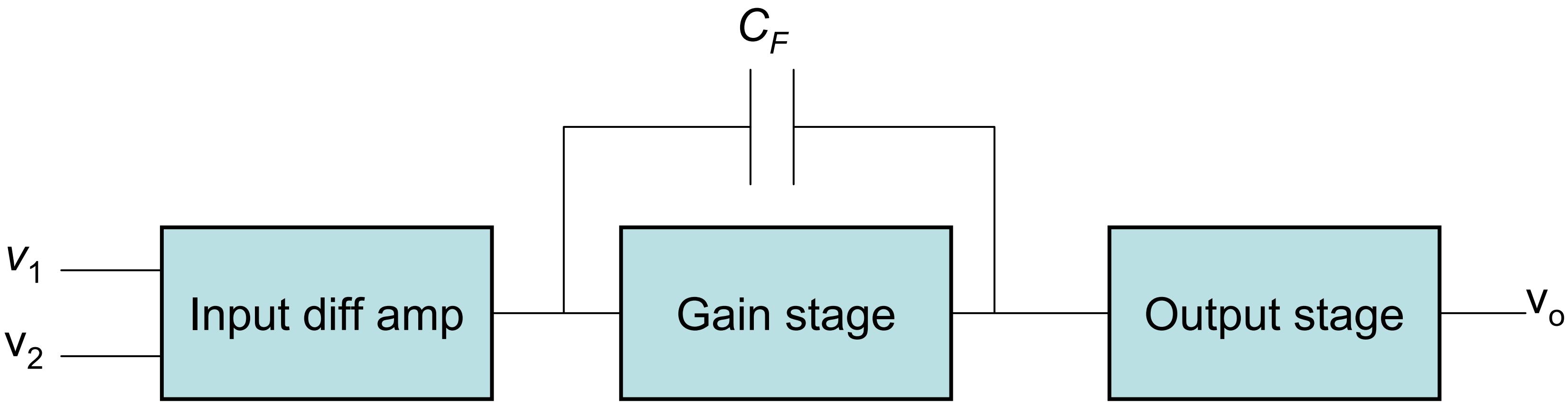
Called operational amplifier due to the use of this amplifier to perform specific electronic circuit functions or operations, such as summation, integration, differentiation, etc.

We studied applications of op amp. Now we analyze and design the circuitry of the op-amp to determine how the various configurations can be combined to form a nearly ideal op amp!

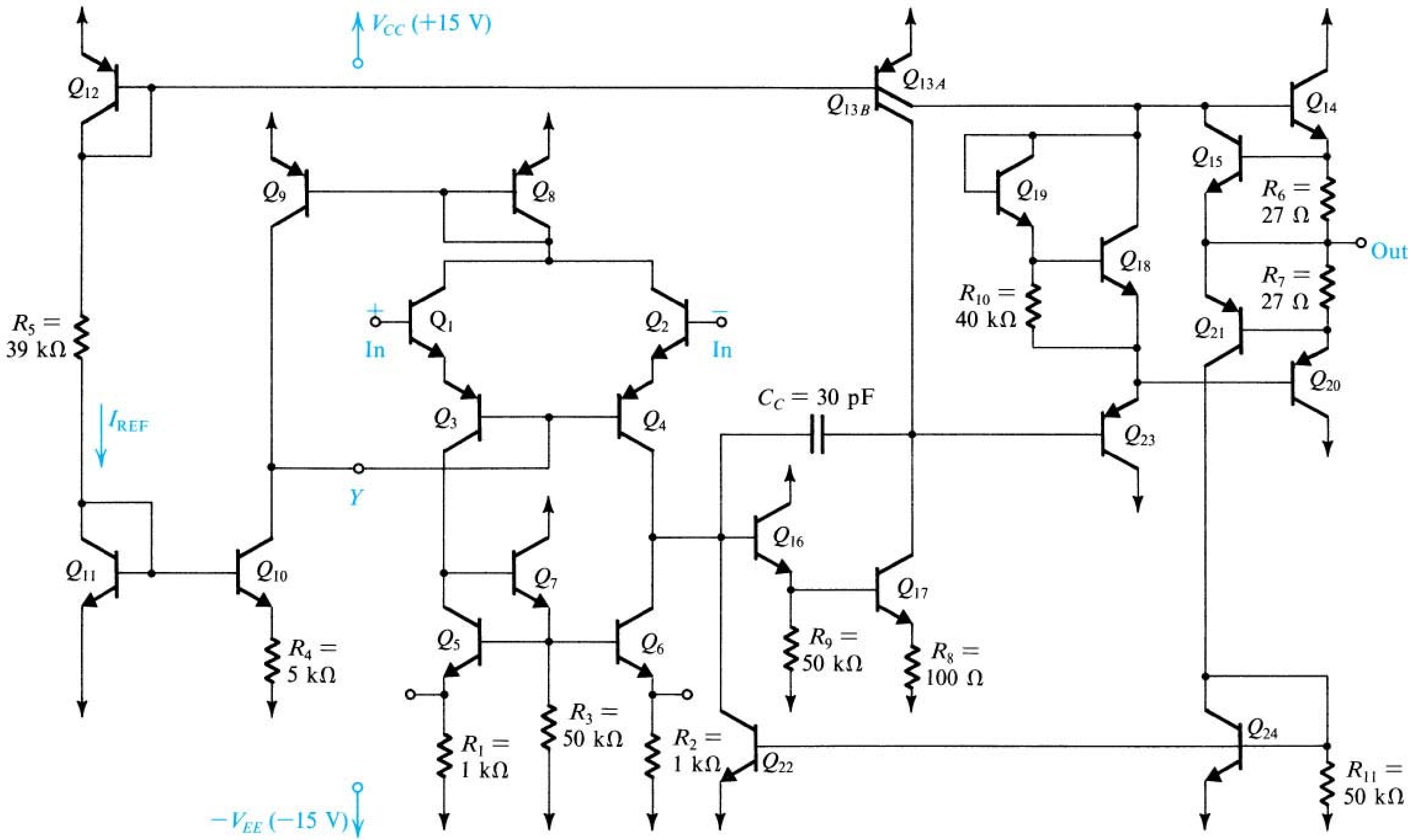
The 741 has been produced since 1966.

The 741 is widely used as general-purpose op-amp

General block diagram of an operational amplifier



The 741 Op-Amp Circuit



Circuit Description

- The 741 consists of three circuits
  - The input differential amplifier (Q_1 through Q_7)
  - The gain stage
  - The output stage (low output resistance)
  - There is also a separate bias circuit, which establishes the bias currents throughout the op amp (Q_8 through Q_{12}).
  - The 741 is biased by both positive and negative supply voltages (typical values $\pm$15 V).
  - The 741 is a DC and small-signal amplifier.
  - The DC output voltage is zero when the applied differential input signal is zero.

Input Differential Amplifier

- Q_1 and Q_2 act as emitter followers causing the input resistance to be high.
- The differential output currents from Q_1 and Q_2 are the inputs to the common-base amplifier formed by Q3 and Q4, which provides a relatively large voltage gain.
- Transistors Q_5, Q_6, and Q_7, with associated resistors R_1, R_2, and R_3 form the active load for the diff amplifier.
- A single sided output at the common collectors of Q_4 and Q_6 is the input signal to the following gain stage.
- The DC output voltage at the collector of Q_6 is at lower potential than the inputs at the bases of Q_1 and Q_2.
- As the signal passes through the op-amp, the DC voltage level shifts several times. By design, when the signal reaches the output terminal, the DC voltage should be zero if a zero differential input signal is applied.

- The two null terminals on the input stage are used to make appropriate adjustment to accomplish this design goal.
- The DC current biasing is initiated by transistors Q_{12} and Q_{11} and resistor R_5.
- Transistor Q_{11} and Q_{10}, with resistor R_4 form a Wildar current source that establishes the bias currents in the common-base transistors Q_3 and Q_4 as well as the current mirror formed by Q_9 and Q_8.
- Q_3 and Q_4 are pnp transistors. They provide added protection against voltage breakdown.

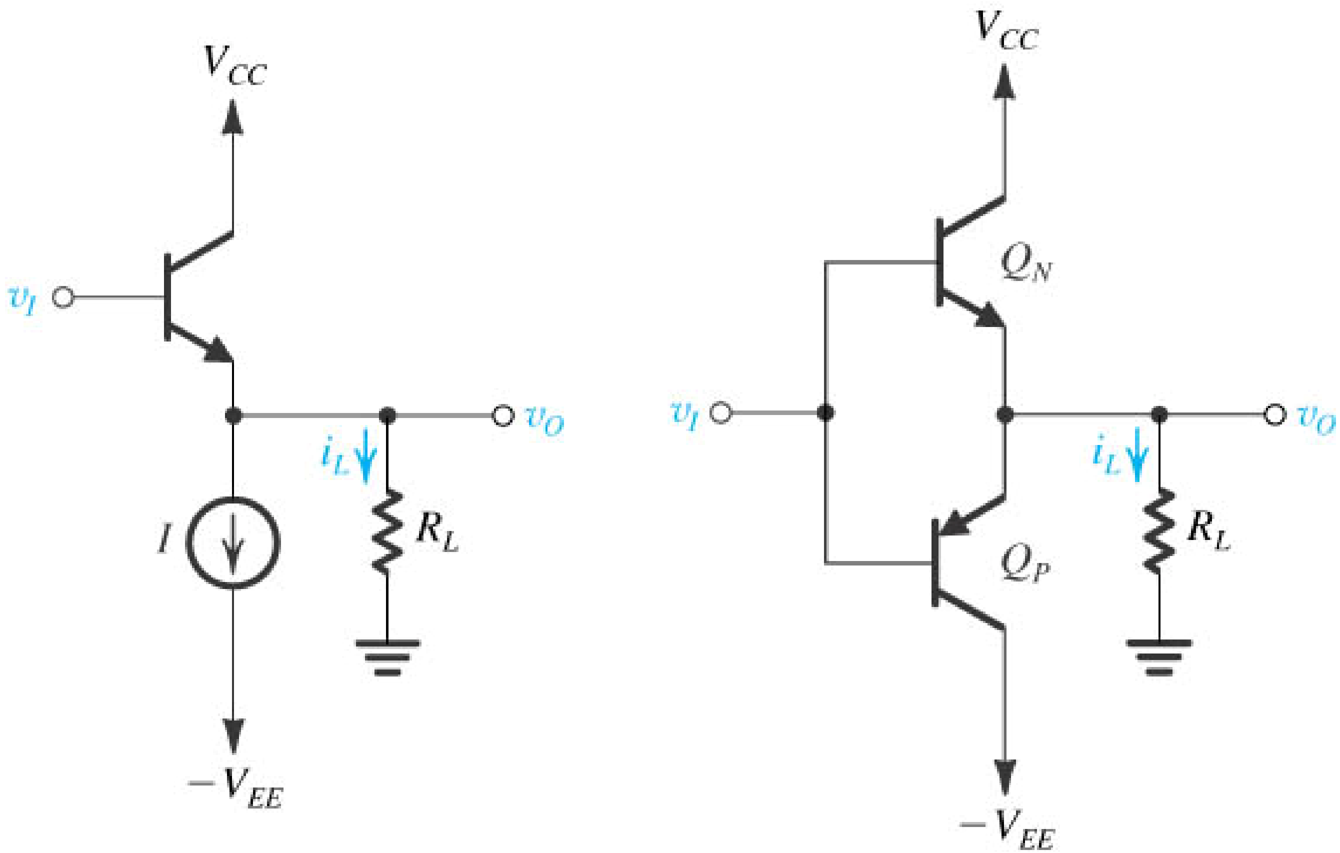
Gain Stage

- The second, or gain, stage consists of transistors Q_{16} and Q_{17}.
- Transistor Q_{16} operates as an emitter follower (high input resistance).
- Q_{13} is effectively two transistors connected in parallel with common base and emitter terminals. The area of Q_{13A} is effectively one-fourth the area of Q_{12}, and the area of Q_{13B} is effectively three-fourths that of Q_{12}.
- Transistor Q_{13B} provides the bias current for Q_{17} and also acts as an active load to produce high voltage gain.
- Transistor Q_{17} operates in a common-emitter configuration.
- The voltage at the collector of Q_{17} is the input signal to the output stage.
- C_C acts as a feedback capacitor between the output and input terminals of the gain stage.

Output Stage

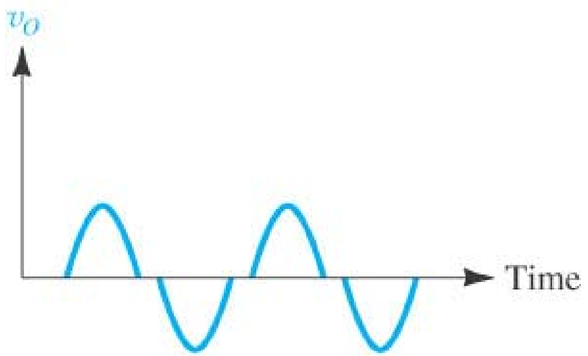
- The output stage of an op-amp provides a low output resistance as well as current gain. It is a class AB circuit with the emitter follower pair Q_{14} and Q_{20}.
- The output of the gain stage is connected to the base of Q_{22}, which operates as an emitter follower and provides a very high input resistance.
- Transistor Q_{13A} provides a bias current for Q_{22}, Q_{18} and Q_{19}.
- Transistors Q_{15} and Q_{21} are referred to as short-circuit protection devices. They are normally off; they conduct only if the output is connected to the ground, resulting in a very large output current.

(a) The emitter follower (b) Class B Output Stage

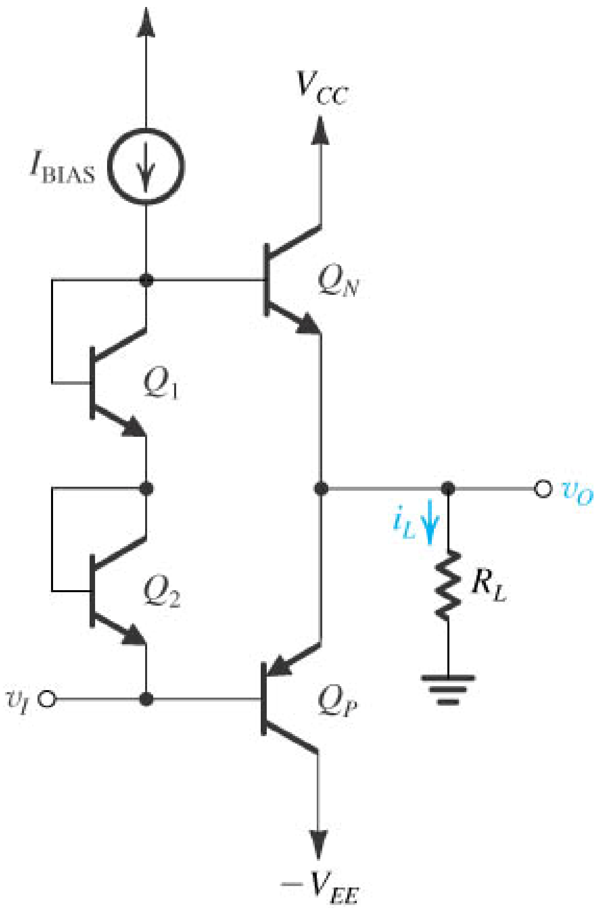


(a) (b)

The output of a class B output stage fed with an input sinusoid



(c)

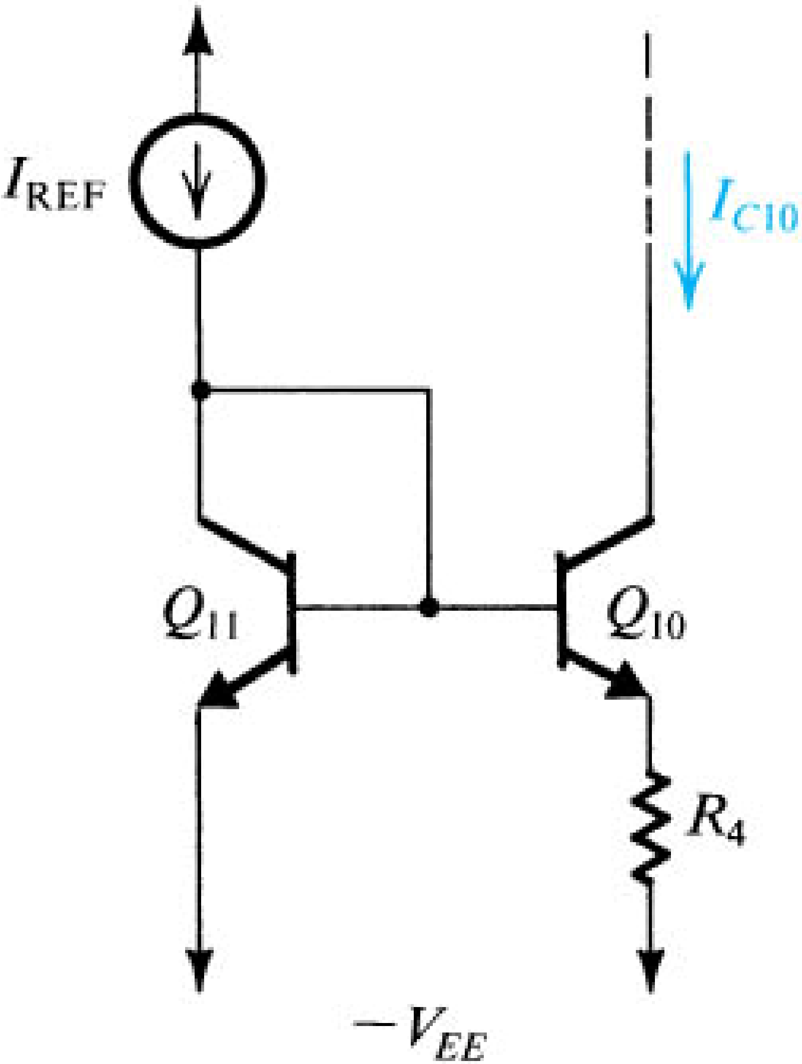


(d)

DC Analysis

- The bias portion of the Op Amp circuit must be identified. A reference current must be calculated and then the bias currents in the individual building blocks of the overall circuit can be determined.
- To determine the DC bias current:
  - We assume both the non-inverting and inverting input terminals are at ground potential and that the DC supply voltages are $\pm$15 V.
  - We may assume V_{BE} = 0.7 V.
- In most DC calculation we may ignore DC base currents.

The DC Analysis of the 741 input stage

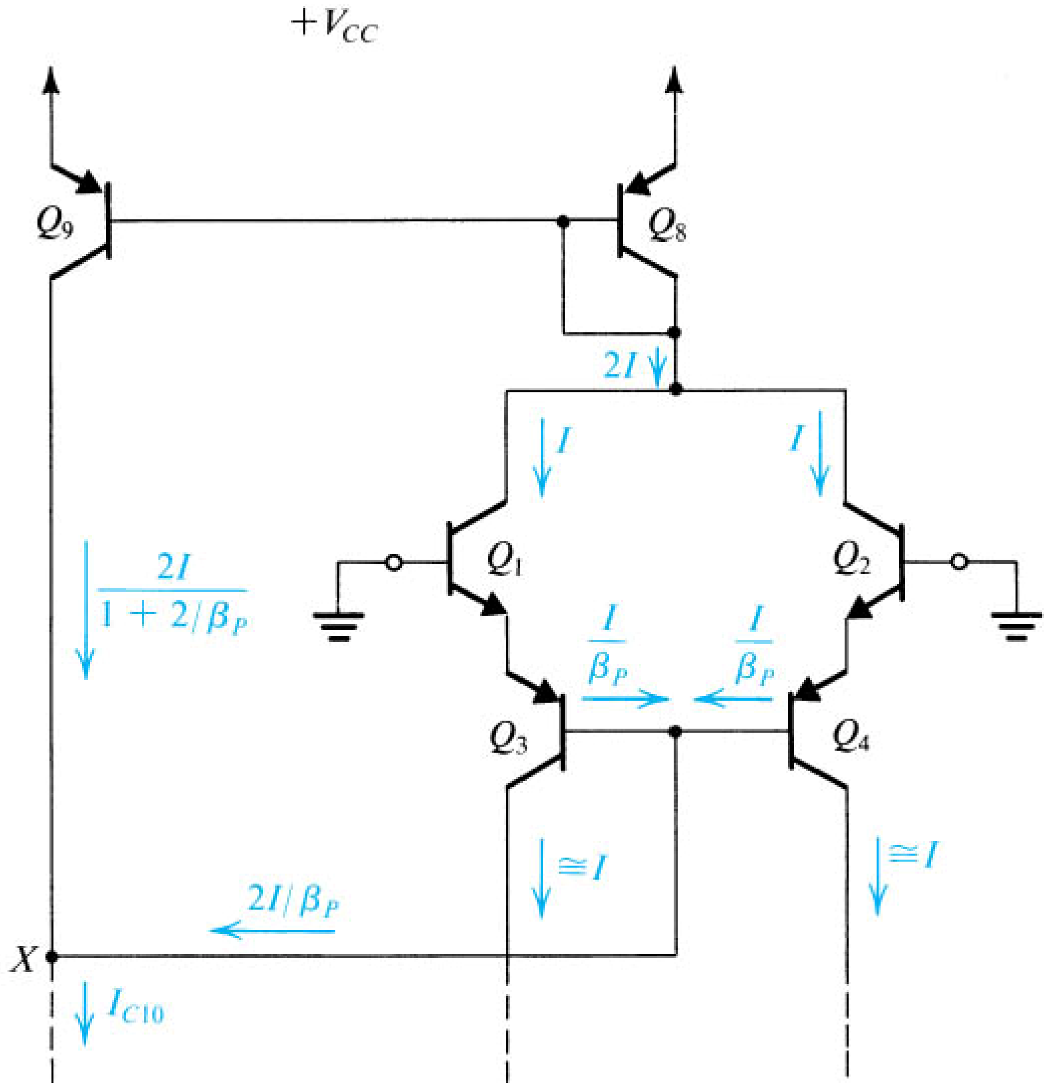


$$I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}$$

$$V_{BE11} - V_{BE10} = I_{C10} R_4$$

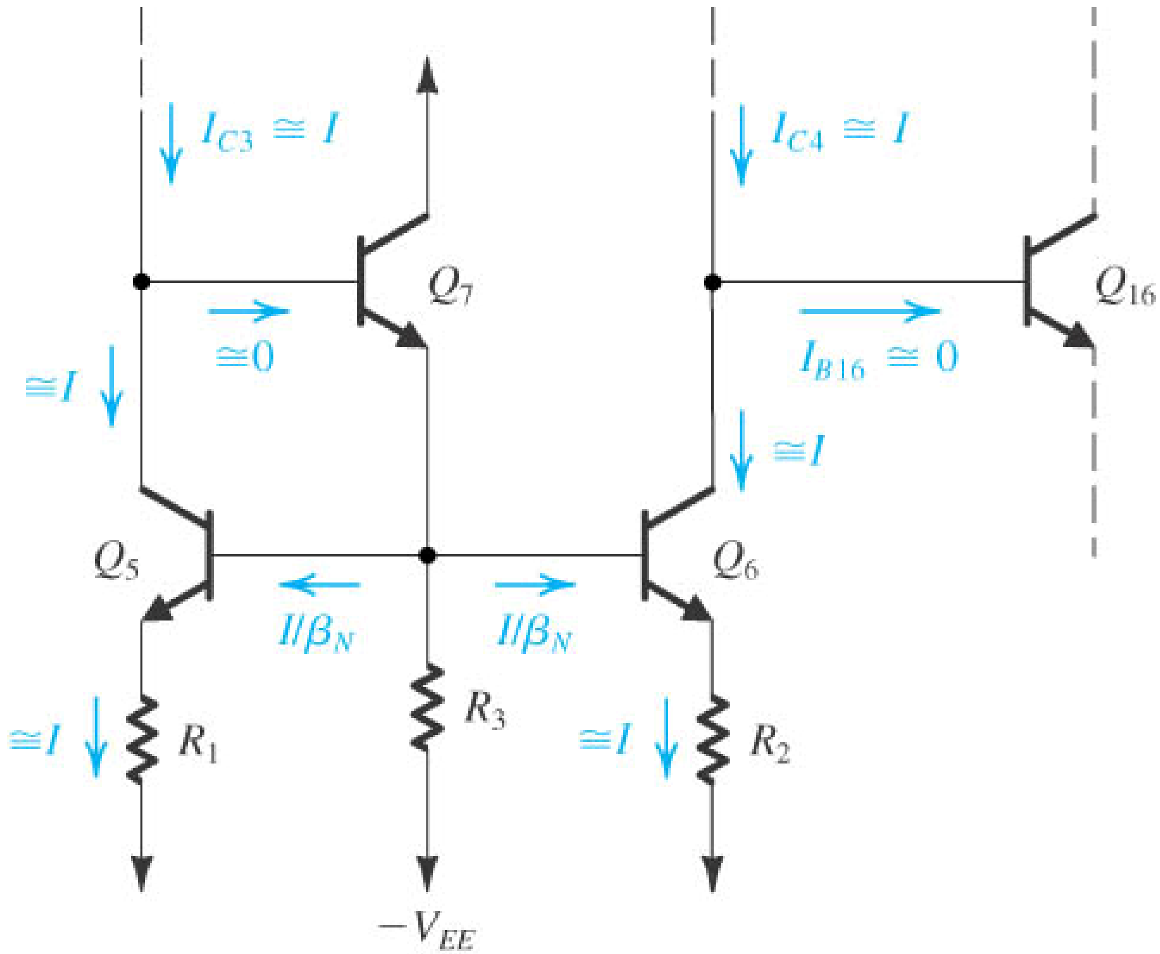
$$V_T \ln \frac{I_{REF}}{I_{C10}} = I_{C10} R_4$$

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = \frac{I_{C10}}{2}$$



+V_CC
Q9
Q8
2I
I
I
Q1
Q2
2I / (1 + 2/β_P)
I/β_P
I/β_P
Q3
Q4
≅I
≅I
2I/β_P
X
I_C10

The AC Analysis of the 741 Input Stage

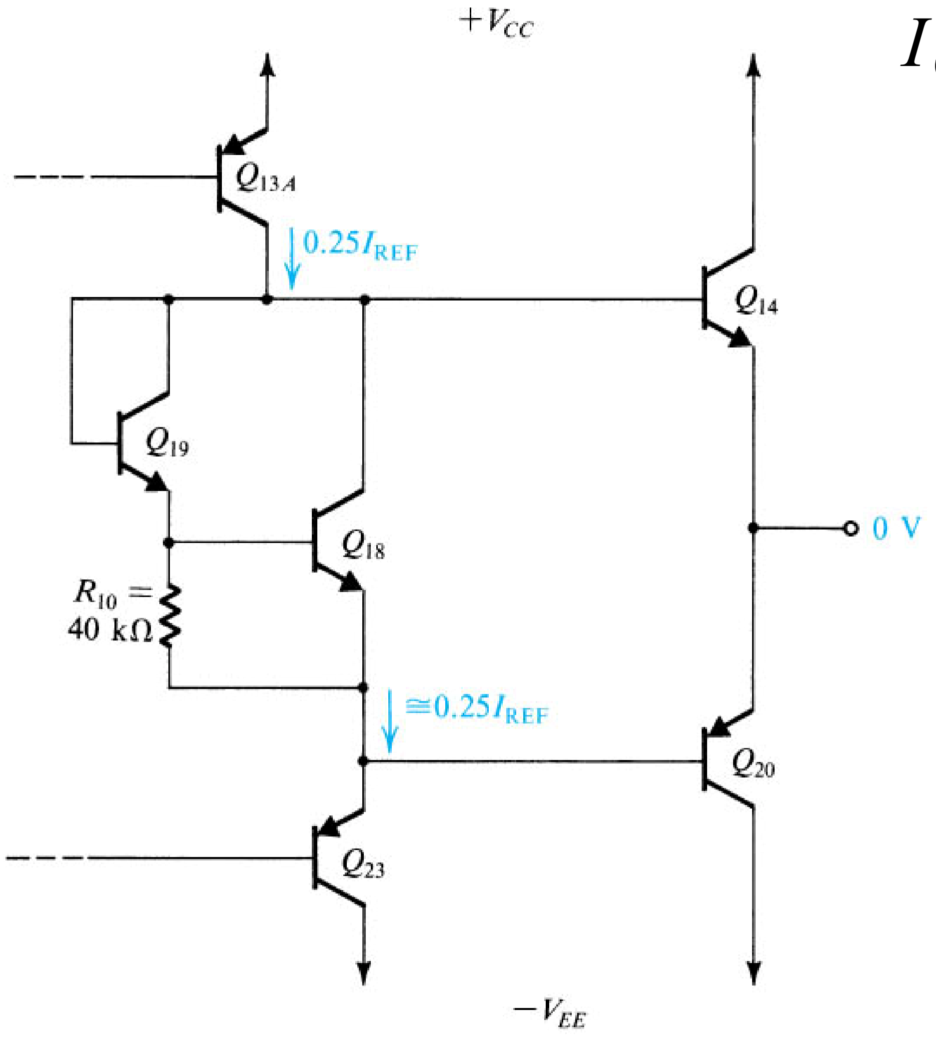


Gain Stage

$$IC_{13B} = 0.75 I_{REF}$$

$$I_{C16} = I_{E16} = I_{B17} + \frac{I_{E17} R_8 + V_{BE17}}{R_9}$$

Output Stage



$$I_{C13A} = 0.25 I_{REF} = I_{Bias}$$

$$I_{C18} = \frac{V_{BE19}}{R_{10}}$$

$$I_{C19} = I_{Bias} - I_{C18}$$

Short Circuit Protection Device

- Resistor R_6 and transistor Q_{15} limit the current in Q_{14} in the event of a short circuit.
- If the current in Q_{14} reaches 20 mA, the voltage drop across R_6 is 540 mV, which is sufficient to bias Q_{15} in the conducting stage.
- As Q_{15} turns on, excess base current into Q_{14} is shunted through the collector of Q_{15}. The base current into Q_{14} is then limited to a maximum value, which limits the collector current.
- The maximum current in Q_{20} is limited by components R_7, Q_{21}, and Q_{24} in much the same way.